A Low-Power 20 GHz Static Frequency Divider with Programmable Input Sensitivity

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Abstract — A low-power frequency divider (divide-by-8) is described which operates up to frequencies in excess of 20 GHz with a supply voltage of 2.7 V. The circuit is implemented in a standard bipolar Silicon technology with a maximum f_T of 37 GHz. The total power dissipation is 57 mW, with 11 mW dissipated in the first divider stage. An innovative implementation of a Toggle flip-flop enables the input sensitivity to be adapted as a function of the input frequency, extending the operation range with respect to standard techniques. An AC simulation model for evaluation of the high frequency performance as a function of design parameters is introduced.

I. Introduction

Frequency- and phase-locking of oscillators in the frequency range from 10 GHz to 20 GHz is a requirement in emerging wireless broadband consumer systems. For example, DVB-RCS satellite return channel transmitters rely on 13.5 GHz oscillators to up-convert the user information to an output frequency range from 29.5 GHz to 30 GHz [1]. To be cost-effective, the locking scheme should preferably be implemented in a low-cost, readily available Silicon technology, and operate at a low power dissipation level.

In this paper we describe a low-power frequency divider (divide-by-8) which operates up to frequencies in excess of 20 GHz. The circuit was implemented in the Philips QUBiC4 technology [2], which provides self-aligned double-poly NPN transistors with a maximum f_T of 37 GHz. Five metalization layers are available, with parasitic capacitances minimized by the use of shallow and deep trench isolation.

Due to an innovative circuit implementation the divider input sensitivity can be adapted as a function of the input frequency, extending the operation range with respect to standard techniques. The divider can be readily used as a building block in PLL frequency synthesizer schemes, for example, to interface Ku-band Dielectric Resonator Oscillators (DRO) to existing, low-cost 2 GHz frequency synthesizers for cellular applications.

II. Circuit design

The prescaler consists of an input amplifier, of a cascade of three divide-by-two stages, and of an output buffer with 50 Ω output impedance for simple interfacing to PCB microstrip lines.

A. Input amplifier

In our design the main function of the input amplifier is not to increase the sensitivity at low input levels, but instead to enable operation with *high* single-ended input levels at high input frequencies. (For an illustration of the problem see, for example [3]). We expanded the upper limit of the sensitivity curve with a single-ended to differential converter design which provides a differential output signal with low DC offset at high input signal levels. The increased input signal range at high frequencies enables, for example, a less critical interfacing of DROs to the divider input.

B. Divider cell

The divider cells are based on the Toggle flip-flop approach. The Toggle flip-flop consists of two D-latches in series, with the inverted output of the second latch being fed-back to the input of the first latch, see Figure 1. A standard Current-Mode-Logic (CML) D-latch consists of a "gate" differential pair (the "gate pair") and of a cross-coupled differential pair (the "latch pair"). The maximum operation frequency of the Toggle flip-flop is determined to a great extent by the load on the output of the gate differential pairs [4]. Figure 1 shows that the output of a gate pair is loaded by the latch pair and by the input circuitry of the other gate pair.

A well-known technique to decrease the load is to add emitter-follower transistors (buffers) in between the output of the gate pairs and the inputs of the latch pair and the gate pair of the other D-latch [3, 4, 5]. This is a proven approach to raise the maximum operation frequency of the Toggle flip-flop, however at the expense of a higher supply voltage and a (significant) higher power dissipation. The use of emitter-followers was not an option for our design,

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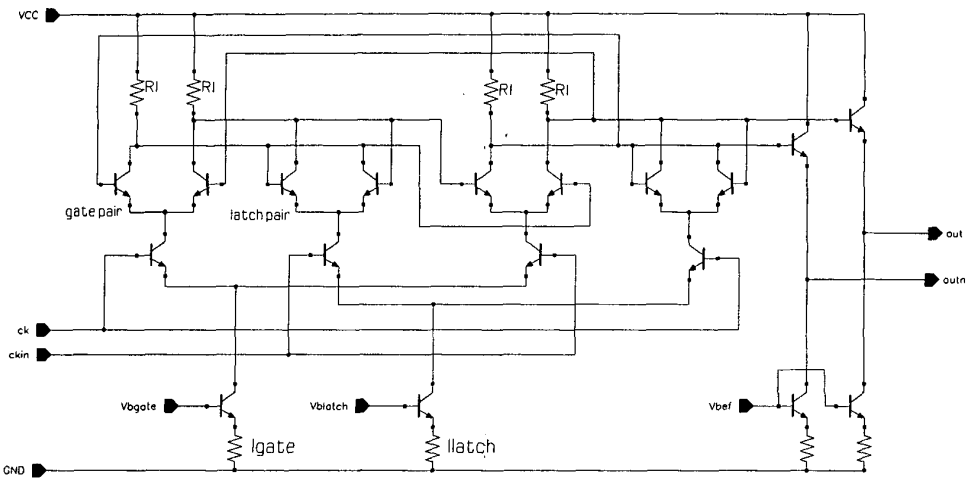

Figure 1. Circuit implementation of an adaptive divider-by-2 cell (adaptive Toggle flip-flop).

due to a low supply voltage specification of 2.7 V and a minimum specified operation temperature of −40°C.

An analysis of the load at the output of a gate pair shows that a latch pair accounts for a significant fraction of the load. At the relatively high current density levels used to achieve peak f_T in the transistors, the dominant parasitic elements of the latch pair are the base-emitter diffusion capacitances, followed by the base-emitter and the collector-substrate junction capacitances. The junction capacitances can be decreased by sizing of the latch pair transistors. A decrease of the base-emitter diffusion capacitances can be achieved with a decrease of the current flowing in the latch pair. However, standard D-latch implementations [3, 4, 5] provide little freedom in that respect, as the gate and latch differential pairs share the same biasing current source.

In our circuit we splitted the biasing currents of the gate and latch pairs as depicted in Figure 1. This enables the bias current of the latch pairs I_{latch} to be set independently of the gate pair biasing current I_{gate}, and a decrease of the latch pair parasitic junction capacitances can be achieved by choice of a smaller transistor size. A smaller biasing current I_{latch} decreases the base-emitter diffusion capacitances of the latch pair, providing a higher maximum operation frequency of the Toggle flip-flop. In fact, at high frequencies the "memory function" of the latch pairs is taken over by the capacitive parasitics present in the circuit, which then perform a "dynamic memory function" [6]. At low frequencies the current I_{latch} can be increased to improve the low-frequency sensitivity level, if that proves necessary for the intended application. In this way the divider described here features a programmable input sensitivity capability. The influence of the biasing current I_{latch} on the high frequency performance will be qualitatively exemplified in the next section.

III. Simulation of High-Frequency Performance

The observation that logical functions implemented with fully differential CML techniques behave in a fairly analog way at high frequencies led us to devise an AC method for assessment of the high-frequency performance. The simulation technique is illustrated in Figure 2. In a small signal analysis carried out with the clock (*ck*) input in balanced state the D-latches of Figure 1 may be seen as two differential amplifiers in cascade. V_{in} is the small signal AC input source, hence V_{out}/V_{in} is the small signal open-loop transfer function of the cascade of two D-latches. The smaller loading of D-latch2's $\bar{Q}$ output, due to the elimination of the connection to the input of D-latch1, is compensated by a "load block" which generates the nominal loading conditions to D-latch2.

The maximum toggle frequency of the flip-flop is proportional to the open-loop bandwidth f_{0dB} of the equivalent "analog system" [7], with f_{0dB} equal to the frequency where $|V_{out}/V_{in}| = 1$. Consequently, a circuit having a larger bandwidth will operate at higher frequencies. Simulation results are presented in Figure 3, showing the open-loop bandwidth f_{0dB} of the cascaded D-latches as a function of the gate pair biasing current I_{gate} and the latch pair biasing current I_{latch}.

Note that we are considering the output circuitry of the Toggle flip-flop. Due to the nature of the division-by-2 operation, we need to multiply the results of Figure 3 by two when referring to the input of the flip-flop. Figure 3

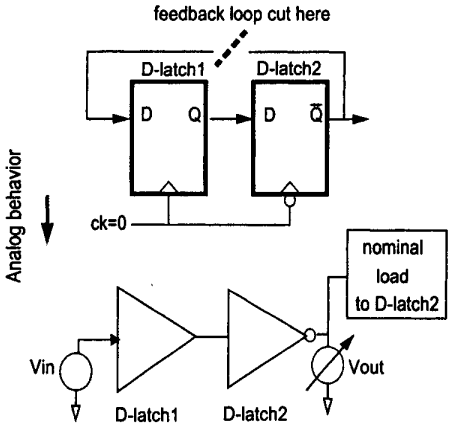

Figure 2. AC simulation model for evaluation of high frequency performance.

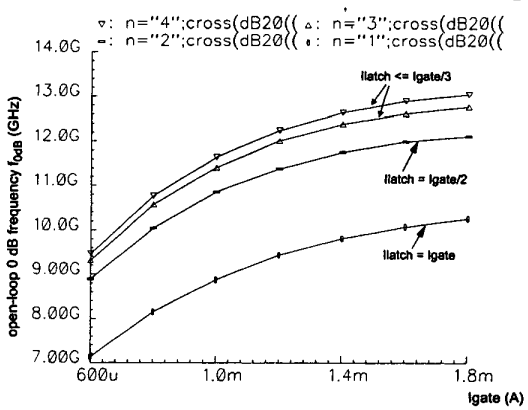

Figure 3. Open-loop 0 dB frequency f_{0dB} of a cascade of two D-latches as a function of the bias currents I_{gate} and I_{latch}, for a fixed value of the logic swing $I_{gate} \times R_l$.

predicts that at the peak f_T current $I_{gate} = 1.2$ mA the maximum operation frequency increases from about 18 GHz for the standard implementation where $I_{latch} = I_{gate}$ to a maximum of nearly 24 GHz with $I_{latch} \leq I_{gate}/3$.

The results of transient simulations are shown in Figure 4. The lower graph shows the waveform at the output of the first Toggle flip-flop for values of $I_{latch} = I_{gate}$ and $I_{latch} = I_{gate}/2$. It can be observed that $I_{latch} = I_{gate}/2$ provides a faster circuit response for the input signal S_{in}. In fact, with $I_{latch} = I_{gate}$ the latch pair strongly pulls the signal in the "wrong direction."

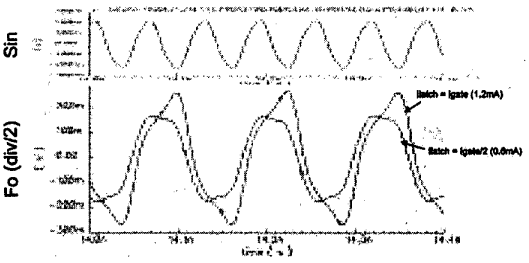

Figure 4. Output signal of the first divider-by-2 as a function of the latch current level. Input frequency = 16 GHz. I_{gate} = 1.2 mA.

IV. Measurements

Measurements of the processed frequency divider test-chips have been performed on-wafer. The biasing currents I_{gate} and I_{latch} can be set externally through input pads. The results of on-wafer sensitivity measurements are presented in Figure 5, for four different situations of I_{latch}, with $I_{gate} = 1.2$ mA. Decreasing I_{latch} increases the maximum operation frequencies as discussed in the previous sections. Note the shift in the free-running oscillation frequencies as well. With $I_{latch} \leq 400\mu$A the gain of the latch pair becomes smaller than 1 and the the divider operates in "dynamic mode." High sensitivity at both ends of the sensitivity curve can be obtained by making I_{latch} adaptive as a function of the operation frequency.

The first divider cell consumes nominally 4 mA, the second and third cells 2 mA each. The input amplifier 4 mA, and the 50 Ω output buffer 8 mA. The total current consumption is therefore 20 mA. With a nominal supply voltage of 2.7 V, the total power dissipation is 57 mW, with 11 mW dissipated in the first divider stage. The low-power dissipation and the high ratio $f_{max,in}/f_T$ = 20 GHz/37 GHz = 0.55 demonstrate the suitability of the adaptive architecture and of the design approach presented here. A micrograph of the adaptive divider test-chip is presented in Figure 6. The size of the active circuitry is 90 μm × 390 μm.

V. Conclusions

A low-power frequency divider (divide-by-8) was described which operated up to frequencies in excess of 20 GHz with a supply voltage of 2.7 V. The circuit was implemented in a standard bipolar Silicon technology with a maximum f_T of 37 GHz. The total power dissipation was 57 mW, with 11 mW dissipated in the first divider stage. An innovative implementation of a Toggle flip-flop enabled the input sensitivity to be adapted as a function of the input frequency, extending the operation range with respect to standard techniques.

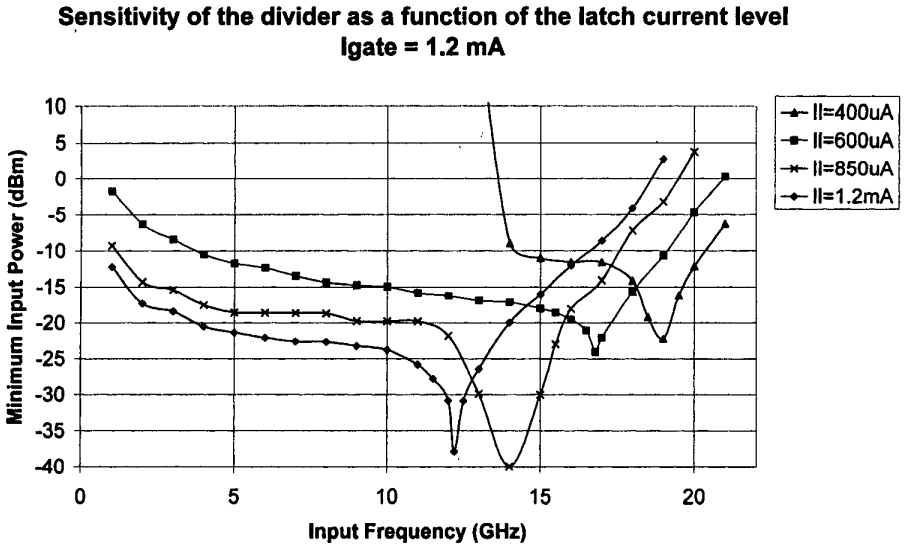

Figure 5. Input sensitivity as a function of the latch current level. On-wafer measurements. I_{gate} = 1.2 mA, I_{amp} = 2 mA, I_{total} = 20 mA, Vcc = 2.7 V.

ACKNOWLEDGEMENTS

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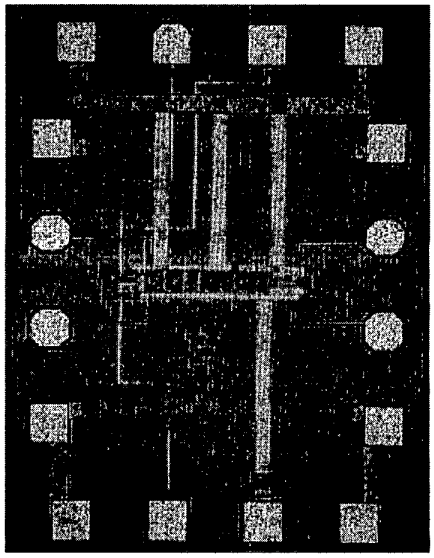

Figure 6. Micrograph of the adaptive divider.